Claims

[c1] What is claimed is:

1. A method of tuning an integrated circuit on an integrated circuit chip comprising:

performing a drain current at saturation measurement of one or more test field effect transistors on said integrated circuit chip;

selectively programming fuses of a bank of fuses on said integrated circuit chip based on said drain current at saturation measurement; and

tuning an operation of said integrated circuit based on a pattern of blown and un-blown fuses in said bank of fuses.

[c2] 2. The method of claim 1, wherein said test field effect transistors are P-channel field effect transistor, N-channel field effect transistors or both P-channel and N-channel field effect transistors.

[c3] 3. The method of claim 1, wherein said one or more test N-channel field effect transistors and said one or more test P-channel field effect transistors include devices selected from the group of devices consisting of design nominal channel length devices, shorter than design nominal channel length devices, longer than design nominal channel length devices, nominal threshold voltage devices, higher than design nominal threshold voltage devices, lower than design nominal threshold devices, nominal gate dielectric thickness devices, thicker than design nominal gate dielectric devices, thinner than design nominal gate dielectric devices and combinations thereof.

[c4] 4. The method of claim 1, further including performing drain current at

aturation measurements on additional one or more test field effect transistors distributed about said integrated circuit chip and selectively programming additional banks of fuses on said integrated circuit chip.

[c5] 5. The method of claim 4, wherein said one or more test field effect transistors and said additional one or more test field effect transistors are located in the corners of said integrated circuit chip.

[c6] 6. The method of claim 4, wherein said one or more test field effect transistors is located in a core containing said integrated circuit to be tuned.

[c7] 7. The method of claim 1, wherein said fuses are selected from the group consisting of laser blow fuses, electrical blow fuses and electrical blow antifuses.

[c8] 8. The method of claim 1, further including the step of selecting which fuses to program based on a lookup table of lists of measured drain currents at saturation versus a corresponding predetermined list of fuse blow patterns.

[c9] 9. The method of claim 1, wherein said tuning of said integrated circuit includes tuning selected from the group of consisting of N-channel field effect off chip driver impedance tuning, P-channel field effect off chip driver impedance tuning, noise to speed ratio off chip driver tuning, data valid window output tuning, core timing tuning and DLL jitter control tuning.

[c10] 10. The method of claim 1, further including selecting one of said one or

more test field effect transistors at a time to perform said drain current at saturation measurement on.

[c11] 11. An electronic device comprising:
a drain current at saturation measurement circuit;
a corresponding bank of fuses; and
means for tuning an output of an integrated circuit to be tuned based upon drain current at saturation measurements encoded in a pattern of blown and un-blown fuses in said fuse bank.

[c12] 12. The electronic device of claim 11, wherein said drain current at saturation measurement circuit includes one or more test P-channel field effect transistors, one or more test N-channel field effect transistors or one or more one or more test P-channel field effect transistors and one or more N-channel field effect transistors.

[c13] 13. The electronic device of claim 12 further including means for selecting one N-channel test field effect transistor or P-channel field effect transistor at a time to perform said drain current at saturation measurement on.

[c14] 14. The electronic device of claim 12, wherein said one or more test N-channel field effect transistors and said one or more test P-channel field effect transistors include devices selected from the group of devices consisting of design nominal channel length devices, shorter than design nominal channel length devices, longer than design nominal channel length devices, nominal threshold voltage devices, higher than design nominal threshold voltage devices, lower than design nominal threshold

devices, nominal gate dielectric thickness devices, thicker than design nominal gate dielectric devices, thinner than design nominal gate dielectric devices and combinations thereof.

[c15] 15. The electronic device of claim 11, further including means for generating a control signal for tuning said integrated circuit based on said pattern of blown and un-blown fuses in said fuse bank.

[c16] 16. The electronic device of claim 11, further including additional drain current at saturation measurement circuits distributed about said integrated circuit chip and additional corresponding banks of fuses.

[c17] 17. The electronic device of claim 16, wherein said drain current at saturation measurement circuit and said additional drain current at saturation measurement circuits are located in the corners of an integrated circuit chip.

[c18] 18. The electronic device of claim 11, wherein said drain current at saturation measurement circuit is located in a core containing said integrated circuit to be tuned.

[c19] 19. The electronic device of claim 11, wherein fuses of said bank of fuses are selected from the group consisting of laser blow fuses, electrical blow fuses and electrical blow antifuses.

[c20] 20. The electronic device of claim 11, wherein said means for tuning said integrated circuit includes tunes the impedance on an output pad of an N-channel field effect off chip driver impedance tuning, tunes the impedance of a P-channel field effect off chip driver, adjusts the ratio of

noise to speed of an off chip driver, adjusts the width of a data valid window of an output circuit, tunes the internal timing of a core timing tuning or adjusts jitter of a delayed lock loop circuit.

[c21] 21. A method of tuning an integrated circuit on an integrated circuit chip comprising:

providing a drain current at saturation measurement circuit on said integrated circuit chip;

providing a corresponding bank of fuses on said integrated circuit chip; and

tuning an output of said integrated circuit based upon said drain current at saturation measurements made using said drain current at saturation measurement circuit encoded in a pattern of blown and un-blown fuses in said fuse bank.

[c22] 22. The method of claim 21, wherein said drain current at saturation measurement circuit includes one or more test P-channel field effect transistors, one or more test N-channel field effect transistors, or one or more one or more test P-channel field effect transistors and one or more N-channel field effect transistors.

[c23] 23. The method of claim 22 further including selecting one N-channel test field effect transistor or P-channel field effect transistor at a time to perform said drain current at saturation measurement on.

[c24] 24. The method of claim 22, wherein said one or more test N-channel field effect transistors and said one or more test P-channel field effect transistors include devices selected from the group of devices consisting

of design nominal channel length devices, shorter than design nominal channel length devices, longer than design nominal channel length devices, nominal threshold voltage devices, higher than design nominal threshold voltage devices, lower than design nominal threshold devices, nominal gate dielectric thickness devices, thicker than design nominal gate dielectric devices, thinner than design nominal gate dielectric devices and combinations thereof.

[c25] 25. The method of claim 21, further including generating a control signal for tuning said integrated circuit based on said pattern of blown and un-blown fuses in said fuse bank.

[c26] 26. The method of claim 21, further including providing additional drain current at saturation measurement circuits distributed about said integrated circuit chip and additional corresponding banks of fuses.

[c27] 27. The method of claim 26, wherein said drain current at saturation measurement circuit and said additional drain current at saturation measurement circuits are located in the corners of an integrated circuit chip.

[c28] 28. The method of claim 21, wherein said drain current at saturation measurement circuit is located in a core containing said integrated circuit to be tuned.

[c29] 29. The method of claim 21, wherein fuses of said bank of fuses are selected from the group consisting of laser blow fuses, electrical blow fuses and electrical blow antifuses.

[c30] 30. The method of claim 21, wherein said tuning of said output of said integrated circuit includes tuning selected from the group of consisting of N-channel field effect off chip driver impedance tuning, P-channel field effect off chip driver impedance tuning, noise to speed ratio off chip driver tuning, data valid window output tuning, core timing tuning and delayed lock loop jitter control tuning.